

Having thus described our invention, what we claim as new, and desire to secure by Letters Patent is:

Sub B1 1 1. A high speed DRAM, comprising:
2 a DRAM memory;
3 a cache memory;
4 a read register coupled between the cache memory and the DRAM
5 memory, for transferring data from the cache memory to the DRAM memory;
6 a write register coupled between the DRAM memory and the cache
7 memory, for transferring data from the DRAM memory to the cache memory;
8 a first bi-directional data bus set coupled between the cache memory
9 and both the read register and the write register;
10 a second data bus set coupled between the read register and the DRAM
11 memory;
12 a third data bus set coupled between the DRAM memory and the write
13 register.

1 2. The high speed DRAM of claim 1, wherein the cache memory
2 comprises a single port SRAM.

Sub B1 1 3. The high speed DRAM of claim 1, wherein a multiplexer couples
2 the cache memory to either of the read register or the write register, and a fourth data
3 bus couples the multiplexer to the read register, and a fifth data bus couples the
4 multiplexer to the write register.

Sub A1 1 4. The high speed DRAM of claim 1, wherein a sixth data bus couples
2 the read register to a data output from the circuit, and a seventh data bus couples a data
3 input to the circuit to the write register.

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1 5. The high speed DRAM of claim 4, wherein an eighth data bus
2 couples the write register to outside data buses.

1 6. The high speed DRAM of claim 5, wherein a multiplexer switches
2 between inputs received from the sixth data bus from the read register and the eight
3 data bus from the write register, and outputs data onto a ninth data bus coupled to the
4 outside data buses.

1 7. The high speed DRAM of claim 6, wherein a read buffer couples the
2 read register to the DRAM memory through a tenth data bus.

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1 8. The high speed DRAM of claim 7, wherein an eleventh data bus
2 couples the DRAM memory to the write buffer which is coupled through the third data
3 bus to the write register.

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1 9. The high speed DRAM of claim 7, wherein the first, second, third,
2 fourth, fifth, tenth, and eleventh data buses all have the same first wide data
3 bandwidth.

1 10. The high speed DRAM of claim 6, wherein the sixth, seventh,
2 eighth, and ninth data buses all have the same second narrow data bandwidth;

1 11. The high speed DRAM of claim 1, wherein data flows through the
2 bi-directional bus in a first direction from the cache memory to the read register, and
3 data flows through the bi-directional bus in a second opposite direction from the write
4 register to the cache memory, such that opposite direction data flows share the same
5 bi-directional data bus in different cycles.

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1 12. The high speed DRAM of claim 1, wherein data flows from the
2 read register to the DRAM memory in a first cycle, and data flows from the DRAM
3 memory to the write register in a second cycle, to share access to the DRAM memory
4 in different cycles.

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1 13. A method of operating the high speed DRAM of claim 1, wherein
2 for a read miss operation, a new set of data are retrieved from the DRAM memory to
3 replace old data in the cache memory, and also to be sent to outside data buses through
4 an output read buffer, and during a first cycle of data flow, data flows from the cache
5 memory through the first and fourth buses and is latched into the read register, and
6 data coming from the DRAM memory are latched into the write register through the
7 third bus, and in a second cycle, the directional flows of the data are reversed through
8 the first and fourth buses and also through the third bus.

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1 14. A method of operating the high speed DRAM of claim 1, wherein
2 for a write miss operation, a new set of data are written into the cache memory to
3 replace retired data, partly from outside data buses via a write buffer, and the rest of
4 the data are from the DRAM memory, and these data are merged in the write register.

1 15. A method of operating the high speed DRAM of claim 1, wherein
2 for a read hit operation, data are transferred nondestructively from the cache memory
3 through the read register to an output read buffer via a multiplexer, and according to a
4 column address, only a portion of the data are transferred to outside data buses.

1 16. A method of operating the high speed DRAM of claim 1, wherein
2 for a write hit operation, a new set of data is transferred to the cache and overwrite a
3 portion of the old data therein.

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1 17. A method of operating the high speed DRAM of claim 1, wherein
2 for a two cycle read hit operation, data that resided in the cache memory are read out
3 according to row address and are latched into the read register based upon column
4 address, and only a portion of these data are transferred to outside data buses via the
5 multiplexer and an output read buffer, and
6 in a first clock cycle, data are latched in sense amplifiers of the cache
7 memory, and
8 in a second clock cycle, data are latched and decoded in the read
9 register.

1 18. A method of operating the high speed DRAM of claim 1, wherein
2 for a two cycle write hit operation, upon detecting a write address is in the cache
3 memory, data is transferred from outside data buses to the cache memory, these data
4 flow via an output write buffer and are then latched into the write register and only
5 occupy a portion of the write register, and only this portion is written into the cache
6 memory based upon column address, and the rest of the data in the same row of the
7 cache memory is maintained unchanged,
8 in a first clock cycle, data are written into the write register, and
9 in a second clock cycle these data are latched into sense amplifiers of
10 the cache memory.

1 19. A method of operating the high speed DRAM of claim 1, wherein
2 for a three cycle read miss operation, upon detecting that read data are not resident in
3 the cache memory, then old data with the same row address are written back into the
4 DRAM memory in a fast cycle DRAM operation wherein original data are destroyed
5 after they are read into the cache memory, and therefore when these data are not
6 needed in the cache memory, they are written back to the DRAM memory to prevent a
7 data loss.

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1 20. A method of operating the high speed DRAM of claim 1, wherein
2 for a three cycle write miss operation, upon detecting that write data address is not
3 resident in the cache memory, then old data in the same row of the cache memory are
4 written back into the DRAM memory, and
5 in a first cycle, old data are latched in sense amplifiers in the cache
6 memory while new data are latched in DRAM memory sense amplifiers and a set of
7 the new data are latched into the write register, and
8 in a second cycle, old data are transferred to the read register, and at the
9 same time new data are transferred from the DRAM memory to the write register,
10 wherein based on the column address, data from the DRAM memory and a set of data
11 from outside data buses are merged,
12 in a third cycle, old data are transferred and latched into the DRAM
13 memory while new data are sent to the cache memory.

1 21. A method of operating the high speed DRAM of claim 1, wherein
2 for a write back operation, which is needed for both a read miss operation and a write
3 miss operation while old data are written back to the DRAM memory, a new set of
4 data from the DRAM memory with a correct row address is read into the write register
5 and then to the cache memory to replace the old data, while retrieving these data, a
6 portion of the data are read to outside data buses based upon column address, decoding
7 is performed in the write register, a selected set of data are transferred to the outside
8 data buses via an output read buffer, wherein two streams of data are transferred
9 simultaneously in two opposite paths via two sets of bus sets,
10 in a first clock cycle, old data are latched into the cache memory sense
11 amplifiers, while new data are latched in the DRAM memory sense amplifiers,
12 in a second cycle, old data are latched into the read register while new
13 data are latched into the write register, and at the same time a set of the data are sent to
14 the outside data buses and are latched into a read buffer,

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in a third cycle, old data are written back into the DRAM memory, and

16 new data from the DRAM memory are transferred into the cache memory to replace

17 old data.